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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/556,777	04/25/2000	Akira Goda	0039-7692-2S	8088
22850	7590	12/16/2003	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			SOWARD, IDA M	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/556,777

Applicant(s)

GODA ET AL.

Examiner

Ida M Soward

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-10, 15-18 and 26-68 is/are pending in the application.
- 4a) Of the above claim(s) 6-10 and 15-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 26-68 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☒ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicants' request for reconsideration filed August 19, 2003 and the interview conducted on September 23, 2003.

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the **second element isolation region** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 26, 45, 47-48 and 50 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The **second element isolation region** is not in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 26, 29, 38, 42, 45-46, 49, 53, 62 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figures 1-2D in view of Huang (5,893,741) and Hayakawa et al. (5,766,996).

In regard to claims 29, 38, 42, 45-46, 49, 62 and 66 and as best understood, Admitted Prior Art Figures 1-2D teach a nonvolatile memory device, comprising: a semiconductor substrate 101 having a peripheral circuit region and a memory cell region; a first element region provided in the peripheral circuit region; a second element region provided in the memory cell region; a first element isolation region (page 2, lines 5-10) provided in the semiconductor substrate, the first element isolation region isolating the first element region; a first transistor having source and drain diffusion layers 106'

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each provided in the first element region; a second transistor having source and drain diffusion layers 106' each provided in the second element region; an insulating film 105 covering the first and second transistors and first element isolation region; and a third transistor having source and drain diffusion layers each provided in the second element region; erasable, programmable memory cell and selection gate transistors (page 1, lines 20-24); an inter-level insulating film 107 provided on the insulating film, the inter-level insulating film containing another insulator different from the insulating film; a contact hole provided in the inter-level insulating film and the insulating film, and contact hole reaching at least one of the source and drain diffusion layers; and a contact 110 provided in the contact hole, the contact electrically connected to the at least one of the source and drain layers; the insulating film is an etch stop of the contact hole, wherein the width is wider than the width of an element region (Figure 1, memory cell region). However, Admitted Prior Art Figures 1-2D fail to teach an insulating film being harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film, and the insulating film being oxidized. Huang teaches an insulating film being oxidized (cols. 2-3, lines 66-67 and 1-17, respectively). Hayakawa et al. teach an insulating film 11, which contain silicon nitride, being harder for an oxidizing agent to pass therethrough, compared with a silicon oxide film (Figure 1(h), cols. 3-4, lines 21-67 and 1-27); another insulating film 11 provided under the insulating film 8 and over the first and second transistors and over isolation regions, the another insulating film containing another insulator different from the insulating film (Figure 1h, cols. 3-4, lines 21-67 and 1-27, respectively). Since Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. are

from the same field of endeavor (semiconductor devices), the purpose disclosed by Hayakawa et al. would have been recognized in the pertinent art of Admitted Prior Art Figures 1-2D and Huang. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the nonvolatile semiconductor memory device of Admitted Prior Art Figures 1-2D by incorporating the oxidized insulating film of Huang and the another insulating film of Hayakawa et al. to prevent the interlayer insulating layer from being oxidized more than necessary (abstract).

Claims 27 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figures 1-2D, Huang (5,893,741) and Hayakawa et al. (5,766,996) as applied to claims 26, 29, 38, 42, 45-46, 49, 53, 62 and 66 above, and further in view of Yatsuda et al. (5,348,898).

Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. teach all mentioned in the rejection above. However, Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. fail to teach oxidized gate electrodes. Yatsuda et al. teach an oxidized gate electrode (col. 26, lines 9-14 and 24-29). Since Admitted Prior Art Figures 1-2D, Huang, Hayakawa et al. and Yatsuda et al. are from the same field of endeavor (semiconductor devices), the purpose disclosed by Yatsuda et al. would have been recognized in the pertinent art of Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the nonvolatile semiconductor memory

device of Admitted Prior Art Figures 1-2D, the oxidized insulating film of Huang and the another insulating film of Hayakawa et al. by incorporating the oxidized gate electrode of Yatsuda et al. to increase gate insulation voltage (col. 26, lines 37-42).

Claims 28 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figures 1-2D, Huang (5,893,741) and Hayakawa et al. (5,766,996) as applied to claims 26, 29, 38, 42, 45-46, 49, 53, 62 and 66 above, and further in view of Saito et al. (4,467,452).

Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. teach all mentioned in the rejection above. However, Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. fail to teach an insulating film having a thickness of at most 50 nm. Saito et al. teach an insulating film 66 having a thickness ranging from 40 to 60 nm (col. 6, lines 53-62), which falls within the range of at most 50 nm. Since Admitted Prior Art Figures 1-2D, Huang, Hayakawa et al. and Saito et al. are from the same field of endeavor (semiconductor devices), the purpose disclosed by Saito et al. would have been recognized in the pertinent art of Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the nonvolatile semiconductor memory device of Admitted Prior Art Figures 1-2D, the oxidized insulating film of Huang and the another insulating film of Hayakawa et al. by incorporating the insulating film thickness of Saito et al. to provide a nonvolatile memory device with an excellent storage retention time (col. 3, lines 47-50).

Claims 30-31 and 54-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figures 1-2D, Huang (5,893,741) and Hayakawa et al. (5,766,996) as applied to claims 26, 29, 38, 42, 45-46, 49, 53, 62 and 66 above, and further in view of Tseng (5,731,130).

Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. teach all mentioned in the rejection above. However, Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. fail to teach an oxidized silicon nitride film, wherein a thickness of the oxidized region of the silicon nitride film is at least 1 nm and at most 10 nm. Tseng teaches an oxidized silicon nitride film, wherein a thickness of the oxidized region of the silicon nitride film is at least 1 nm and at most 10 nm (col. 8, lines 42-49). Since Admitted Prior Art Figures 1-2D, Huang Hayakawa et al. and Tseng are from the same field of endeavor (semiconductor devices), the purpose disclosed by Tseng would have been recognized in the pertinent art of Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the nonvolatile semiconductor memory device of Admitted Prior Art Figures 1-2D, the oxidized insulating film of Huang and the another insulating film of Hayakawa et al. by incorporating the oxidized silicon nitride film of Tseng to the limitation of alignment tolerances (col. 2, lines 48-52).

Claims 32-33 and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figures 1-2D, Huang (5,893,741) and Hayakawa

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et al. (5,766,996) as applied to claims 26, 29, 38, 42, 45-46, 49, 53, 62 and 66 above, and further in view of Yokoi et al. (4,866,003).

Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. teach all mentioned in the rejection above. However, Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. fail to teach a hydrogen containing silicon nitride film having a concentration of at most 3×10^{21} atoms/cm³. Yokoi et al. teach a hydrogen containing silicon nitride film 12 having a concentration of at most 3×10^{21} atoms/cm³ (col. 3, lines 37-41). Also, it is well known in the semiconductor art for the concentration of an impurity to be higher at the surface and decreases deeper into the material. Since Admitted Prior Art Figures 1-2D, Huang, Hayakawa et al. and Yokoi et al. are from the same field of endeavor (semiconductor devices), the purpose disclosed by Yokoi et al. would have been recognized in the pertinent art of Admitted Prior Art Figures 1-2D, Huang Hayakawa et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the nonvolatile semiconductor memory device of Admitted Prior Art Figures 1-2D, the oxidized insulating film of Huang and the another insulating film of Hayakawa et al. by incorporating the hydrogen containing silicon nitride film of Yokoi et al. to provide a semiconductor device which is free from the deterioration in device characteristics due to hot carriers by having a reduced amount of hydrogen in the silicon nitride (col. 2, lines 9-12).

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Claims 34-37, 39-41, 43-44, 58-61, 63-65 and 67-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figures 1-2D, Huang (5,893,741) and Hayakawa et al. (5,766,996) as applied to claims 26, 29, 38, 42, 45-46, 49, 53, 62 and 66 above, and further in view of Ma (US 6,211,548 B1).

Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. teach all mentioned in the rejection above. Admitted Prior Art Figures 1-2D further teach a gate electrode of each of the first and second transistors is a stacked gate structure including a floating gate 103a and a control gate 103c, wherein the floating gate of the selection gate transistor is electrically connected to the control gate of the selection gate transistor and the gate electrode of the erasable and programmable memory cell transistor is a stacked gate structure including a floating gate and a control gate. However, Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. fail to teach a metal or metal silicide gate electrode, wherein the metal contains tungsten. Ma teaches a metal or metal silicide gate electrode, wherein the metal contains tungsten (claim 16). Since Admitted Prior Art Figures 1-2D, Huang, Hayakawa et al. and Ma are from the same field of endeavor (semiconductor devices), the purpose disclosed by Ma would have been recognized in the pertinent art of Admitted Prior Art Figures 1-2D, Huang and Hayakawa et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the nonvolatile semiconductor memory device of Admitted Prior Art Figures 1-2D, the oxidized insulating film of Huang and the another insulating film of Hayakawa et al. by incorporating the a metal or metal silicide gate

electrode of Ma to significantly reduce wordline RC delay without any die area penalty (col. 4, lines 9-11).

Response to Arguments

Applicant's arguments with respect to claims 26-68 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to semiconductor devices having an oxidized insulating film:

Ema (5,405,798)

Park et al. (US 6,498,097 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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November 5, 2003



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